10/Appeal Brief 4-8-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	DAVID W. WU MICHAEL P. DUANE SCOTT D. LUNING	§	**Group Art Unit:**	2814
Serial No.:	09/784,629	§		
Filed:	February 15, 2001	§	**Examiner:**	P. Cao
Title:	SEMICONDUCTOR DEVICE AND METHOD FOR LOWERING MILLER CAPACITANCE FOR HIGH-SPEED MICROPROCESSORS	§	**Docket No.**	2000.032100/TT3633

BOX AF
Assistant Commissioner for Patents
Board of Patent Appeals & Interferences
Washington, D.C. 20231

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First-Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on the date below:
March 27, 2003 Kathy Navas
Date Signature

APPEAL BRIEF

Dear Sir:

Applicant hereby submits an original and two copies of this Appeal Brief to the Board of Patent Appeals and Interferences in response to the final rejection mailed on January 2, 2003.

Enclosed is a check in the amount of $320.00 to cover cost for filing this Appeal Brief. If the check is inadvertently omitted, or should any additional fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason relating to the enclosed materials, or should an overpayment be included herein, the Assistant Commissioner is authorized to deduct or credit said fees from or to Advanced Micro Devices, Inc.'s Deposit Account No. **01-365/TT3633.**

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I. REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc. The assignment of the present application to Advanced Micro Devices, Inc., is recorded at Reel 11602, Frame 0831.

II. RELATED APPEALS AND INTERFERENCES

Applicant is not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

Claims 1-20 and 47 have been finally rejected and the rejection of these claims is the subject of this appeal. More specifically:

claims 1-7, 11-17, and 47 were rejected under 35 U.S.C. 102(b) as being anticipated by Thompson, et al (U.S. Patent No. 6,020,244); and

claims 8-10 and 18-20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson, et al (U.S. Patent No. 6,020,244) in view of Son, et al (U.S. Patent No. 6,103,562).

IV. STATUS OF AMENDMENTS

Claims 1-20 and 47 are pending in the present application. No amendments were made after the Final Office Action mailed on January 2, 2003. The claims as currently pending are attached as Appendix A.

V. SUMMARY OF THE INVENTION

Generally, the present invention relates to a method of reducing Miller capacitance in semiconductor devices. The so-called Miller capacitance typically exists in overlap regions of

semiconductor devices such as overlap regions 135S and 135D (indicated in phantom) in a conventional MOS transistor 100 shown in Figure 1 of the Patent Application. The Miller capacitance tends to reduce the switching speed of semiconductor devices. For example, when the MOS transistor 100 is in an "off" state, there may be some residual charge stored in the drain overlap region 135D, primarily due to the Miller capacitance. This "Miller charge" must be discharged before the MOS transistor 100 may be switched from the "off" state to an "on" state, slowing down the switching speed of the MOS transistor 100. Similarly, the Miller capacitance in the overlap region 135D must be charged up again with the "Miller charge" after the MOS transistor 100 is switched from the "on" state to the "off" state, further slowing down the switching speed. See Patent Application, page 4, ll. 15-23.

To reduce the Miller capacitance, and thereby increase the switching speeds of various semiconductor devices, Applicants describe (and claim in independent claims 1, 11, and 47) forming a gate dielectric above a surface of a substrate, forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region, and forming a first dopant-depleted region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure. With particular regard to independent claim 11, Applicants further describe and claim forming a source/drain extension adjacent the doped-poly gate structure and a dopant-depleted-SDE region in the substrate under the edge region of the doped-poly gate structure.

VI. ISSUES ON APPEAL

The issues on appeal are as follows:

A. Are claims 1-7, 11-17, and 47 anticipated by Thompson, et al (U.S. Patent No. 6,020,244)?

B. Are claims 8-10 and 18-20 unpatentable over Thompson, et al (U.S. Patent No. 6,020,244) in view of Son, et al (U.S. Patent No. 6,103,562)?

VII. GROUPING OF THE CLAIMS

For the issues presented above, claims 1-7, 10-17, 20, and 47 can be considered to stand or fall together, and claims 8-9 and 18-19 can be considered to stand or fall together.

VIII. ARGUMENT

A. Claims 1-7, 11-17, and 47 are not anticipated by Thompson.

The Examiner has admitted that Thompson does not expressly disclose forming a first dopant-depleted region in the edge region of the doped-poly gate structure, as claimed in independent claims 1, 11, and 47. See Final Office Action, page 2, item 2. Nevertheless, the Examiner's position is that the process taught by Thompson inherently forms the first dopant-depleted region in the edge region of the doped-poly gate structure.

Applicants respectfully submit that the Examiner' rejection of claims 1-7, 11-17, and 47 is based upon a misapplication of the principles of inherency. As the Board well knows, inherency in anticipation requires that the asserted proposition *necessarily* flow from the disclosure. *In re Oelrich*, 212 U.S.P.Q. (BNA) 323, 326 (C.C.P.A. 1981); *Levy*, 17 U.S.P.Q.2d (BNA) at 1463-64; *Skinner*, at 1789; *In re King*, 231 U.S.P.Q. (BNA) 136, 138 (Fed. Cir. 1986). It is not enough that a reference could have, should have, or would have been used as the claimed invention. "The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Oelrich*, at 326, quoting *Hansgirg v. Kemmer*, 40 U.S.P.Q. (BNA) 665, 667 (C.C.P.A. 1939); *In re Rijckaert*, 28 U.S.P.Q.2d (BNA) 1955, 1957 (Fed. Cir. 1993), quoting *Oelrich*, at 326; *see also Skinner*, at 1789. "Inherency... may not be established by probabilities or possibilities. The mere fact that a certain thing may

result from a given set of circumstances is not sufficient." *Ex parte Skinner*, 2 U.S.P.Q.2d (BNA) 1788, 1789 (Bd. Pat. App. & Int. 1987), citing *In re Oelrich*, 666 F.2d 578, 581 (C.C.P.A. 1981). Consequently, where anticipation is found through inherency, the Office's burden of establishing *prima facie* anticipation includes the burden of providing "...some evidence or scientific reasoning to establish the reasonableness of the examiner's belief that the functional limitation is an inherent characteristic of the prior art." *Ex parte Skinner*, 2 U.S.P.Q.2d (BNA) 1788, 1789 (Bd. Pat. App. & Int. 1987).

Applying these legal principles to the present case, it is respectfully submitted that the process taught by Thompson does not inherently form the first dopant-depleted region in the edge region of the doped-poly gate structure and, therefore, the present invention is not anticipated by Thompson.

Thompson describes a gate 20 that is formed so that it is insulated from a substrate 30 by an insulative layer 27. Spacers 21 and 22 are then formed along opposite sides of the gate 20 and used to define shallower extensions of the source and drain regions 23, 24. See Thompson, col. 2, ll. 31-42 and Figure 2. A p-type region 25, which is more heavily doped than the substrate 30, is formed between the source and drain regions 23, 24. See Thompson, col. 2, ll. 45-48 and Figure 2. The region 25 is formed by ion implantation at a very high tilt angle using alight dopant species implanted at a relatively high energy. In particular, Thompson teaches implanting ions having an energy level of 10-20 KeV. This is done to force the dopant beneath the gate and into the central region of the channel. See Thompson, col. 3, ll. 11-38 and Figure 3. The Examiner alleges that because of the angled implant of the p-type dopant through the edge regions of the doped-poly gate 20, a dopant-depleted-poly region would inherently be formed in this edge region. See item 2 on pages 2-3 of the Final Office Action.

However, those of ordinary skill in the art will appreciate that the location and/or depth of an implanted dopant is determined, at least in part, by the implant energy of the dopant. In contrast to Thompson, Applicants describe, in one embodiment, implanting a dopant at a relatively low energy, *e.g.* an implant energy ranging from about 0.2-5 keV, in order to form the first dopant-depleted region in the edge region of the doped-poly gate structure adjacent the gate dielectric and the second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure. This implant energy limitation is specifically set forth in dependent claims 8-9 and 18-19. Thus, it is respectfully submitted that the formation of the first dopant-depleted region in the edge region of the doped-poly gate structure adjacent the gate dielectric and the second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure does not necessarily flow from the process disclosed by Thompson, where the dopants are implanted at a relatively high energy, such as an energy level of 10-20 KeV, to force the dopant beneath the gate and into the central region of the channel.

The Examiner has attempted to rebut this argument by stating at item 5 on page 5 of the Final Office Action that Applicants have not demonstrated that the dopant-depleted regions must not be formed by the process disclosed in Thompson. It is respectfully submitted that the Examiner has misapplied the legal principles of inherency. Contrary to the Examiner's position, the Applicants do not have the burden of showing that the dopant-depleted regions must not be formed by the process disclosed in Thompson. Rather, it is the Examiner's burden to show that the pending claims are anticipated by the prior art, either expressly or under the principle of inherency. *Ex parte Skinner*, (quoted above). Respectfully, the Examiner failed to do that in this case.

As stated above, the mere fact that a certain thing may result from a given set of circumstances is not sufficient to establish inherency. Inherency in anticipation requires that

the asserted proposition necessarily flows from the disclosure. *In re Oelrich*, (cited above). Applicants respectfully submit that the Examiner has not provided any scientific evidence or reasoning to show that the process described by Thompson necessarily forms a dopant-depleted region in the edge region of the gate structure.

For at least the aforementioned reasons, Applicants respectfully submit that the Examiner's rejection of the claims 1-7, 11-17, and 47 as being anticipated by Thompson is improper and based on misapplication of the principle of inherency.

B. Claims 8-10 and 18-20 are not unpatentable over Thompson in view of Son.

The claims should be allowed because the cited prior art does not teach or suggest all of the claim limitations.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable

expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. A teaching in the prior art that the claimed combination is not desirable suggests that there is not a reasonable expectation of success.

The Examiner relies on Son to teach specific counter-dopant concentrations. However, Son does not remedy the aforementioned deficiencies in the primary reference. In particular, Son is completely silent with regard to forming a first dopant-depleted region in the edge region of the doped-poly gate structure adjacent the gate dielectric and the second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure.

Furthermore, the cited references do not teach or suggest implanting the counter-dopant at an implant energy ranging from about 0.2-5 keV, as specifically set forth in dependent claims 8-9 and 18-19. Thompson teaches implanting a dopant at an energy range that greatly exceeds the range taught in the present invention. In particular, Thompson teaches implanting a dopant at a relatively high energy, such as an energy level of 10-20 KeV. Thompson also provides no motivation for implanting the dopant at an implant energy ranging from about 0.2-5 keV because that is counter to Thompson's stated intent to force the dopant beneath the gate and into the central region of the channel. Son is completely silent with regard to the implant energy.

For at least the aforementioned reasons, Applicants respectfully submit that the Examiner's rejection of the claims 8-10 and 18-20 as being obvious over Thompson in view of Son is incorrect because the cited references fail to disclose each and every limitation of claims 8-10 and 18-20.

IX. CONCLUSION

In view of the foregoing arguments, Applicant respectfully requests that the board of Patent Appeals and Interferences reverse the decision rejecting claims 1-20 and 47 and direct the Examiner to pass the case to issue.

Respectfully submitted,

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AGENT FOR APPLICANTS

APPENDIX A

The claims on appeal are:

1. A method comprising:

forming a gate dielectric above a surface of the substrate;

forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region; and

forming a first dopant-depleted region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure.

2. The method of claim 1, wherein forming the first_dopant-depleted region includes implanting a counter-dopant into the edge region of the doped-poly gate structure adjacent the gate dielectric, and forming the second dopant-depleted region includes implanting the counter-dopant into the substrate under the edge region of the doped-poly gate structure.

3. The method of claim 2, the method further comprising:

implanting the counter-dopant at an angle α with respect to a direction perpendicular to the surface, wherein the angle α is in a range of about 7°-45°;

rotating the substrate through at least one of approximately 90° (approximately $\pi/2$ radians), approximately 180° (approximately π radians), and approximately 270° (approximately $3\pi/2$ radians); and

implanting the counter-dopant at the angle α with respect to the direction perpendicular to the surface.

4. The method of claim 1, the method further comprising:

forming a photoresist mask defining a source/drain extension (SDE) adjacent the doped-poly gate structure.

5. The method of claim 2, the method further comprising:

forming a photoresist mask defining a source/drain extension (SDE) adjacent the doped-poly gate structure.

6. The method of claim 3, the method further comprising:

forming a photoresist mask defining a source/drain extension (SDE) adjacent the doped-poly gate structure.

7. The method of claim 1, wherein forming the first and second dopant-depleted regions includes depleting the edge region of the doped-poly gate structure adjacent the gate dielectric by forming depleting dielectric spacers adjacent the doped-poly gate structure and depleting the substrate under the edge region of the doped-poly gate structure by forming the depleting dielectric spacers.

8. The method of claim 2, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure and the substrate under the edge region includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure and the substrate under the edge region, a dose of the one of

phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×10^{14} ions/cm^2 to about 1.0×10^{15} ions/cm^2 at an implant energy ranging from about 0.2-5 keV.

9. The method of claim 3, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure and the substrate under the edge region includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure and the substrate under the edge region, a dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×10^{14} ions/cm^2 to about 1.0×10^{15} ions/cm^2 at an implant energy ranging from about 0.2-5 keV.

10. The method of claim 1, wherein forming the first dopant-depleted region in the edge region of the doped-poly gate structure includes forming the first dopant-depleted region to have a depth from the edge of the doped-poly gate structure, the depth of the first dopant-depleted region ranging from about 50 Å-100 Å.

11. A method comprising:

forming a gate dielectric above a surface of a substrate;

forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region;

forming a source/drain extension (SDE) adjacent the doped-poly gate structure; and

forming a dopant-depleted-poly region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a dopant-depleted-SDE region in the substrate under the edge region of the doped-poly gate structure.

12. The method of claim 11, wherein forming the dopant-depleted-poly region includes implanting a counter-dopant into the edge region of the doped-poly gate structure adjacent the gate dielectric, and forming the dopant-depleted-SDE region includes implanting the counter-dopant into the substrate under the edge region of the doped-poly gate structure.

13. The method of claim 12, the method further comprising:

implanting the counter-dopant at an angle α with respect to a direction perpendicular to the surface, wherein the angle α is in a range of about 7°-45°;

rotating the substrate through at least one of approximately 90° (approximately $\pi/2$ radians), approximately 180° (approximately π radians), and approximately 270° (approximately $3\pi/2$ radians); and

implanting the counter-dopant at the angle α with respect to the direction perpendicular to the surface.

14. The method of claim 11, the method further comprising:

forming a photoresist mask defining the SDE adjacent the doped-poly gate structure.

15. The method of claim 12, the method further comprising:

forming a photoresist mask defining the SDE adjacent the doped-poly gate structure.

16. The method of claim 13, the method further comprising:

forming a photoresist mask defining the SDE adjacent the doped-poly gate structure.

17. The method of claim 11, wherein forming the dopant-depleted-poly region includes depleting the edge region of the doped-poly gate structure adjacent the gate dielectric by forming depleting dielectric spacers adjacent the doped-poly gate structure, and forming the dopant-depleted-SDE region includes depleting the SDE in the substrate under the edge region of the doped-poly gate structure by forming the depleting dielectric spacers above the SDE.

18. The method of claim 12, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure, and implanting the counter-dopant into the substrate under the edge region of the doped-poly gate structure includes implanting the one of phosphorus, arsenic, boron and boron fluoride into the substrate under the edge region of the doped-poly gate structure, a dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×10^{14} ions/cm^2 to about 1.0×10^{15} ions/cm^2 at an implant energy ranging from about 0.2-5 keV.

19. The method of claim 13, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure, and implanting the counter-dopant into the substrate under the edge region of the doped-poly gate structure includes implanting the one of phosphorus, arsenic, boron and boron fluoride into the substrate under the edge region of the doped-poly gate structure, a dose of the one of

phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×10^{14} ions/cm^2 to about 1.0×10^{15} ions/cm^2 at an implant energy ranging from about 0.2-5 keV.

20. The method of claim 11, wherein forming the dopant-depleted-poly region in the edge region of the doped-poly gate structure includes forming the dopant-depleted-poly region to have a first depth from the edge of the doped-poly gate structure, the first depth ranging from about 50 Å-100 Å, and forming the dopant-depleted-SDE region in the substrate under the edge region of the doped-poly gate structure includes forming the dopant-depleted-SDE region to have a second depth from the surface of the substrate, the second depth ranging from about 50 Å-100 Å.

47. A method, comprising:

forming a gate dielectric above a surface of a semiconductor substrate;

forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region; and

forming a first dopant-depleted region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure by:

implanting a counter-dopant into the edge region of the doped-poly gate structure adjacent the gate dielectric; and

forming depleting dielectric spacers adjacent the doped-poly gate structure.